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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,931	08/13/2004	Steven Sang	13154-US-PA	4930

31561 7590 07/26/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
WILSON, ALLAN R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,931	SANG, STEVEN	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3-6 and 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,158,899 to Yamagata. Yamagata teaches, with reference to figure 1E, an ESD device comprising:

a first conductive type substrate 2;

a gate structure 5 disposed over the substrate;

a second conductive type source 9 and drain 8 separately disposed in the substrate on each side of the gate structure;

a second conductive type doped layer 3 disposed in the substrate underneath and apart from the source and drain regions; and

a second conductivity type extended doped region 10, disposed in the substrate adjacent to the doped layer and the source region;

wherein, under a circuit connection to the INTERNAL CIRCUIT, the drain region, the substrate and the source region together form a first parasitic BJT (because the drain and source regions are N-type and the substrate P-type and separating the source and drain region, a parasitic BJT is necessarily formed), the drain region, the substrate and the doped layer together

form a second parasitic BJT 11 so that a current flowing into the drain region is channeled to a common voltage terminal (ground or Vcc) via the first and second parasitic BJTs.

Regarding claims 3, 4, 8 and 9, Yamagata teaches in figure 1E that the first conductivity is P-type and the second conductivity is N-type. Yamagata also teaches an embodiment in figure 5 in which the first conductivity is N-type and the second conductivity is P-type. Regarding claims 5 and 10, Yamagata teaches that the gate structure is that of an NMOS which by definition comprises a bottom dielectric and a top conductive layer (col. 6, line 36).

Regarding claims 6 and 11, Yamagata also teaches that the device comprises a plurality of parallel-connected transistors as shown in figure 1E, wherein the two transistors 5 are connected as having a common drain.

2. Claims 1-3, 5-8, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by 6,424,013 to Steinhoff et al. Steinhoff et al. teach, with reference to figure 3B, an ESD device comprising:

a first conductive type substrate 342;

a gate structure 354 disposed over the substrate;

a second conductive type source 350 and drain 352 separately disposed in the substrate on each side of the gate structure;

a second conductive type doped layer 340 disposed in the substrate underneath and apart from the source and drain regions; and

a second conductivity type extended doped region 332, disposed in the substrate adjacent to the doped layer and the source region;

wherein, under a circuit connection to the PROTECED CIRCUIT, the drain region, the substrate and the source region together form a first parasitic BJT 510 (col. 4, lines 35-38) and the drain region, the substrate and the doped layer together form a second parasitic transistor BJT (because the drain and doped layer are N-type and the substrate, which is P-type, is separating the drain and doped layer, a parasitic BJT is necessarily formed), so that a current flowing into the drain region is channeled to a common voltage terminal (ground 126) via the first and second parasitic BJTs.

Regarding claims 2 and 7, Steinhoff et al. teach that the substrate 342, gate 354, source 350 and extended doped region 340 are coupled to ground. Regarding claims 3 and 8, Steinhoff et al. teach that the first conductivity is N-type and the second conductivity is P-type (as shown in figure 3B). Regarding claims 5 and 10, Steinhoff et al. teach that the gate structure is a MOS device which necessarily has a conductive top layer and a dielectric bottom layer. Regarding claims 6 and 11, Steinhoff et al. teach that the device comprises a plurality of parallel-connected transistors (gates 354 denote two transistors), which are connected in a common-drain configuration (col. 3, lines 57-59).

Regarding claims 12 and 13, Steinhoff illustrates in fig. 3B the common voltage is a ground voltage connected via 126.

Response to Arguments

Applicant's arguments filed 06/20/2005 have been fully considered but they are not persuasive.

The argument that "Yamagata (Fig. l E), has shown the structure with only one BJT 11 being created. Therefore, Yamagata does not disclose the ;structure of the present invention to create two parasitic BJT's" is not persuasive. As stated in the rejection "because the drain and doped layer are N-type and the substrate, which is P-type, is separating the drain and doped layer, a parasitic BJT is necessarily formed." One BJT exist between the drain 8, each source 9 and doped layer 3. The other BJT is clearly show as reference no. 11. Therefore, there are two BJT's formed and the rejection stands.

The argument that "with respect to claims 12-13 with defining the common voltage as the ground voltage, when. the ESD current enters the BJT 11 froth the drain region 8, the current is channeled to the system voltage Vcc" is not persuasive. Examiner agrees that Yamagata shows the BJT 11 channels the current to Vcc, however Steinhoff illustrates in FIG. 3B the drain region 352 is channeled to a common voltage terminal (ground 126) via the first parasitic BJT and the second parasitic BJT.

The argument that "Steinhoff does not disclose the second BJT of the present invention" and "[i]n FIG 3B and FIG. 5, clearly, the substrate 338 and the N-type layer 340 are used to create the parasitic capacitor Cpn (326, 314) and the; parasitic diode D1 (324, 3.12). In other words, Steinhoff indeed failed to disclose the second BJT, as recited in claims 1 and 6" is not persuasive. Examiner agrees that a parasitic capacitor Cpn and a parasitic diode D1 are formed by Steinhoff, but two BJT's are also formed. Steinhoff illustrates in FIG. 3B a drain 352, a P-

WELL 338 and a N-BURIED LAYER 340 which form the first parasitic npn BJT. Additionally, FIG. 3B shows the drain, the P-WELL and a source 230 form the second parasitic npn BJT. Therefore, there are two BJT's formed and the rejection is affirmed.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Note: The present application has been transferred to another examiner.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
22 July 2005